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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,362	11/26/2003	Shinsuke Asari	XA-9990	6170

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MILES & STOCKBRIDGE PC
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MCLEAN, VA 22102-3833

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,362	ASARI ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received November 26, 2003 has been considered.

Where the provided translation of a foreign patent publication was limited to the abstract, only the abstract has been considered.

The Japanese foreign reference no. 2002-197876 fails to comply with 37 CFR 1.98(a)(3), because the reference is not in the English language and an explanation of its relevance has not been provided. Therefore this reference has not been considered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Gorobets (US Patent No. 6,898,662).

For claim 1, Gorobets discloses a storage device comprising a nonvolatile memory and a control circuit (a non-volatile memory and a controller, col. 1, lines 59-60),

wherein said nonvolatile memory has a plurality of a plurality of memory blocks, each of which has a plurality of sub memory blocks comprising a plurality of nonvolatile memory cells, and is capable of performing programming to a first sub memory block within a first memory block and a second sub memory block within a second memory block in parallel (a memory system comprising a non-volatile memory and a controller for writing host data to memory and wherein the controller simultaneously initiates concurrent page program or block erase operations in at least two arrays of memory, 58-63), and

wherein said control circuit controls programming to said nonvolatile memory with an address information and data in accordance with being issued from an outside device (the controller of the memory system connects the system to a host via a logical interface, col. 2, lines 51-52).

wherein said first sub memory block of said first memory block includes a management area for storing a management information which includes a linking information between said first sub memory block of said first memory block and corresponding sub memory blocks of other memory blocks (a system write pointer, used

to define the physical location for writing system sectors transmitted by a host system wherein system sectors are identified by their logical address, col. 7, lines 61-64; each block contains data associated with a single pointer, col. 8, lines 7-8), and

wherein said control circuit controls that reading said linking information from said first sub memory block of said first memory block in accordance with said address information, and programming to one or more of said first sub memory block of said first memory block in accordance with said address information and corresponding sub memory blocks of other memory blocks relating to said first memory block by said linking information (the microprocessor controls the flow of data sectors through the memory access control bus of the controller, implements management algorithms which define sectors and control data storage organization, and defines the characteristics of the logical interface to the host, col. 4, lines 20-25; the logical interface to the memory system allows data to be written to and read from the system by sectors, each of which is identified by a logical address, col. 2, lines 55-60).

For claim 2, Gorobets discloses a translation table used for translating from said address information issued from said outside device to a first physical address for selecting said first sub memory block of said first memory block (a sector address table is maintained in memory which includes the physical address for every logical sector. In addition, every sector is written with a header containing its logical address, providing a means of verifying sector identity, col. 9, lines 16-20),

wherein said control circuit reads said linking information from said first sub memory block of said first memory block selected by said first physical address

translated by said translation table from said address information (physical address data updates to specific blocks of the sector address table, col. 9, lines 64-65).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gorobets (US Patent No. 6,898,662), Tomita (US Patent No. 6,901,479) and Arakawa et al (US Patent No. 5,590,073).

For claim 3, Gorobets discloses the invention as per rejection of claims 1-2 above. Gorobets does not, however, expressly disclose a buffer memory capable of storing data supplied from or supplying to an outside device.

Tomita, however, discloses an address translation table for translating the logical address of an effective logical block used by a host into a physical address in a disk array (col. 2, lines 47-50), and a write buffer for storing temporarily the data to be written into a disk array (col. 2, lines 57-59).

The combined teachings of Tomita and Gorobets fail to disclose, storing to said nonvolatile memory when power supplying is turned off, and is storing to said buffer memory when power supplying is turned on.

Arakawa, however, discloses a buffer memory may be comprised of an SRAM, and when power is turned on, data is written into and read from the SRAM. When power is turned off, data is evacuated to nonvolatile memory (col. 3, lines 14-18).

Arakawa, Gorobets and Tomita are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include storing to a nonvolatile memory when power supplying is turned off, and storing to a buffer memory when power supplying is turned on, because this would allow for a nonvolatile memory device to store and hold data without the use of a backup power source (col. 14, lines 57-61), and because the nonvolatile memory may be used as an SRAM during supply of power, and a flash memory when the power is turned off, thereby partially realizing an unlimited writing flash memory (col. 15, lines 5-8), as taught by Arakawa.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gorobets (US Patent No. 6,898,662), Tomita (US Patent No. 6,901,479), Arakawa et al (US Patent No. 5,590,073) and Takata (US PGPub No. 20010036105).

For claim 4, the combined teachings of Gorobets, Tomita, and Arakawa disclose the invention as per rejection of claims 1-3 above. These teachings fail to disclose, however, sub memory blocks are coupled to a word line, and wherein said selecting of said sub memory block is selecting said word line corresponding to said physical address.

Takata, however, discloses each memory cell array block includes a plurality of word lines (par. 0013), and a plurality of memory cell array blocks each include a plurality of nonvolatile memory transistors to which information can be written and from which information can be read and erased, a plurality of word lines each connected to the control gates of these transistors, and a word line selection signal in accordance with a signal level of an input address signal (par. 0026).

Takata, Gorobets, Tomita, and Arakawa are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include selecting of a word line because this would help in preventing data in a memory cell array block to be inadvertently or illegally rewritten (par. 0027), as taught by Takata.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gorobets (US Patent No. 6,898,662), Tomita (US Patent No. 6,901,479), Arakawa et al (US Patent No. 5,590,073), Takata (US PGPub No. 20010036105) and Jeddeloh (US Patent No. 6,052,798).

For claim 5, the combined teachings of Gorobets, Tomita, Arakawa and Takata disclose the invention as per rejection of claims 1-4 above. These teachings fail to disclose, however, said control circuit detects existing an error nonvolatile memory cell in a third sub memory block related by said linking information in said first sub memory block, said control circuit controls changing said linking information replacing said third sub memory block to a forth sub memory block.

Jeddeloh, however, discloses defective memory portions of memory blocks in a memory module are detected and an error map is created which identifies the defective memory portions of the module and uses such to create and store a remapping table that maps each of the defective portions to non-defective portions in the module (col. 2, lines 7-33), and a memory controller determines from the remapping table the non-defective memory portion to which the requested memory portion is mapped, and accesses and performs a function accordingly (col. 4, lines 45-51).

Jeddeloh, Gorobets Tomita, Arakawa and Takata are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include error detection and changing of linking information and replacing accordingly, because this enables memory modules with defective memory locations to be employed in error-sensitive applications (col. 2, lines 33-38), as taught by Jeddeloh.

9. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorobets (US Patent No. 6,898,662), Tomita (US Patent No. 6,901,479), Arakawa et al (US Patent No. 5,590,073), Takata (US PGPub No. 20010036105), Jeddeloh (US Patent No. 6,052,798) and Conley (US Patent No. 6,968,421).

For claim 6, the combined teachings of Gorobets, Tomita, Arakawa, Takata and Jeddeloh disclose the invention as per rejection of claims 1-5 above. These teachings fail to disclose, however, programming to said first sub memory block, said control circuit controls reading data from said first sub memory block, merging data read from

said first sub memory block and new data received from said outside device and programming to a new first sub memory block, a second physical address of which is different from said first physical address of said first sub memory block.

Conley, however, discloses memory cell blocks are divided into multiple pages, and the data from a block that is not being updated needs to be copied from an original block to a new block that also contains the new, updated data being written by a host (col. 5, lines 50-54).

Conley, Gorobets, Tomita, Arakawa, Takata and Jeddeloh are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include merging data read with new data received for sub memory blocks, because this allows more efficient use of the pages of new blocks, and allows the updated data to be stored in any erased pages of the same block as superceded data (col. 3, lines 2-5), as taught by Conley.

For claim 7, the combined teachings of Gorobets, Tomita, Arakawa, Takata, Jeddeloh and Conley disclose the invention as per rejections of claims 1-6 above. Conley further discloses said control circuit controls changing said translation table replacing said first physical address of said first sub memory block to said second physical address of said new first sub memory block as a corresponding physical address of said address information received from said outside device, after programming to said new first sub memory block (partial tables show mapping of the

logical blocks into the original and new physical blocks before and after the updating of data, col. 6, lines 12-21).

Conley, Gorobets, Tomita, Arakawa, Takata and Jeddeloh are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include changing the address of blocks in a translation table to new ones after programming accordingly because this allows data in pages of the block not involved in a write operation but contained in the same physical block as the superceded data to not be copied into a new block (35-38), as taught by Conley.

10. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorobets (US Patent No. 6,898,662), Tomita (US Patent No. 6,901,479), Arakawa et al (US Patent No. 5,590,073), Takata (US PGPub No. 20010036105), Jeddeloh (US Patent No. 6,052,798), Conley (US Patent No. 6,968,421) and Sinclair et al (US Patent No. 6,725,321).

For claim 8, the combined teachings of Gorobets, Tomita, Arakawa, Takata, Jeddeloh and Conley disclose the invention as per rejection of claims 1-7 above. These teachings fail to disclose, however, management information includes a first information which indicates that each of said first sub memory block and said corresponding sub memory blocks of other memory blocks relating to said first memory block by said linking information is already erased or not.

Sinclair, however, discloses a controller is configured to compile a list of the physical block addresses of at least some of the blocks of sectors being treated as erased (col. 3, lines 42-59).

Sinclair, Gorobets, Tomita, Arakawa, Takata, Jeddeloh and Conley are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include erased status indication for memory blocks because this may be used by the controller in order to quickly identify the next block of sectors to be written to (col. 3, lines 49-50), as taught by Sinclair.

For claim 9, the combined teachings of Gorobets, Tomita, Arakawa, Takata, Jeddeloh, Conley and Sinclair disclose the invention as per rejections of claims 1-8 above. Conley further discloses a plurality of volatile memories, wherein each of said volatile memories is corresponding to each of said memory blocks and is capable of storing program data (the table is usually stored in a volatile memory of the controller for ease of access, col. 6, lines 24-25).

Conley, Gorobets, Tomita, Arakawa, Takata, Jeddeloh and Sinclair are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a plurality of volatile memories because this allows for ease of access of the controller (col. 6, lines 25-26), as taught by Conley.

For claim 10, the combined teachings of Gorobets, Tomita, Arakawa, Takata, Jeddeloh, Conley and Sinclair disclose the invention as per rejections of claims 1-9

above. Conley further discloses programming to said first sub memory block, said control device controls reading data from said first sub memory block to said volatile memory corresponding to said first memory block (a portion of the table stored in a volatile memory of the controller is usually formed immediately in advance of a read or programming operation that involves the blocks included in the table portion, col. 6, lines 24-30).

Conley, Gorobets, Tomita, Arakawa, Takata, Jeddeloh and Sinclair are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include programming and reading from sub blocks to a volatile memory because, as stated above, this allows for ease of access for the controller (col. 6, lines 25-26), as taught by Conley.

Citation of Pertinent Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dakhil (US Patent No. 6,748,505) discloses a system bus for shared communication link to communicate control, address, and data information between multiple sub-blocks within a system.

Contact Information

12. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

2-22-06

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